The Thesis Committee for Boyang Zhang
certifies that this is the approved version of the following thesis:

FinFET Standard Cell Optimization for Performance and Manufacturability

APPROVED BY

SUPERVISING COMMITTEE:

David Z. Pan, Supervisor

Nan Sun

FinFET Standard Cell Optimization for Performance and Manufacturability

by

Boyang Zhang, B.E.

THESIS

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Dedicated to my parents.

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I am very fortunate and honored to have Professor David Z. Pan as my Master advisor during my graduate study at the University of Texas at Austin. He is not only an outstanding mentor in academic research, but also helps me realize the purpose of life. I greatly appreciate all the things that I have learned from him, which will benefit the rest of my life.

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I dedicate my thesis to my parents in China. Without their love, encouragement and sacrifice, I would not have been as I am.

FinFET Standard Cell Optimization for Performance and Manufacturability

by

Boyang Zhang, M.S.E
The University of Texas at Austin, 2012

Supervisor: David Z. Pan

As Moore's law continues to 20nm and below, traditional CMOS device faces severe short channel effects. Industry is switching from traditional CMOS to FinFET in order to keep Moore's law alive. Due to the three-dimensional structure of FinFET, many challenges need to be solved. After that, FinFET will finally be able to replace traditional CMOS in the semiconductor industry.

This thesis discusses the manufacturing challenges of FinFET. In addressing these challenges, characterization of the FinFET standard cells has been done. The characterization is based on saturation current, leakage current, implantation angle and the average edge placement error at metal one layer. Three design variables, including the metal pitch, the fin pitch and the fin width are optimized to achieve better design quality. Standard cell library which contains combinatorial cells as well as sequential cells are characterized and optimized. Two optimization scenarios are included in the final results. One is performance driven, optimizing the saturation current and the leakage

current, while the other is manufacturability driven, optimizing the implantation angle and the average EPE. The optimization results show the tradeoff between performance and manufacturability.

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Chapter 1

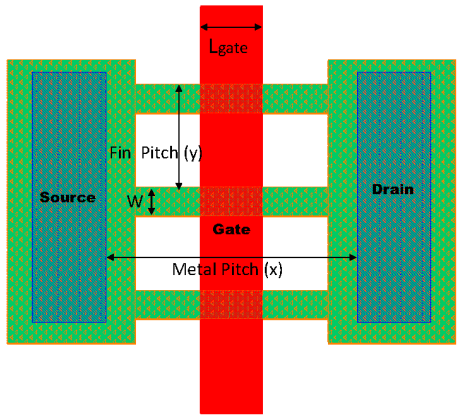
Introduction

FinFET is considered as the substitution device for traditional CMOS. In this chapter, it is pointed out that the transition from traditional CMOS to FinFET is inevitable. In addition, three major manufacturing challenges are described.

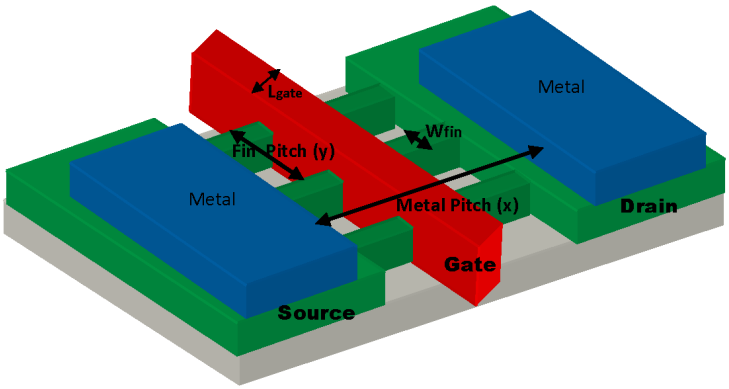
1.1 FinFET for Sub-20 nm

Traditional CMOS scaling faces challenges due to material and process technology limits. Obstacles for scaling planar devices to sub-32nm gate lengths include short-channel effects (SCE), sub-threshold leakage and gate-dielectric leakage.

FinFET is a multi-gate three-dimensional transistor structure [16]. As shown in Fig. 1.1, the silicon "fin" shape channel is surrounded by the gate. As marked in Fig. 1.1, some variables are defined to be used for layout design optimization. The metal pitch x is defined as the distance between the metal strip on the source side and the metal strip on the drain side. The fin width w is defined as the vertical dimension of the fin along the gate direction. The fin pitch y is defined as the distance between two adjacent fins plus the fin width.



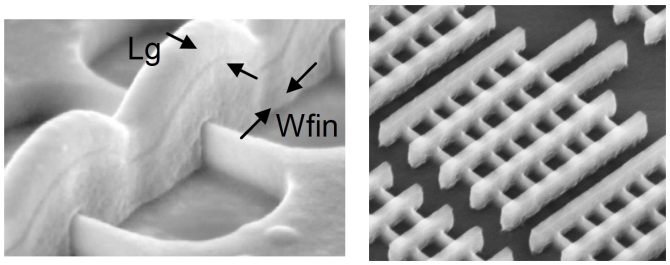
(a)



(b)

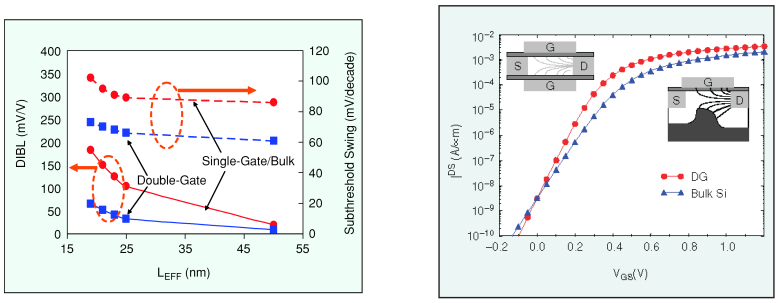
Figure 1.1: FinFET Model. (a)Top view. (b)Three-dimensional view.

For a certain nFET or pFET, the gate length is defined as the length of the fin portion which is covered by the gate. In our model, fin height is not explicitly included due to the two dimensional simulation environment. The longitudinal electric field generated by the drain is better screened from the source due to proximity of the channel, resulting in reduced short-channel effects. This also reduces drain induced barrier lowering (DIBL) and improves sub-threshold



(a) (b)

Figure 1.2: FinFET SEM photos. (a)Fabricated FinFET [20]. (b)Source: Intel.



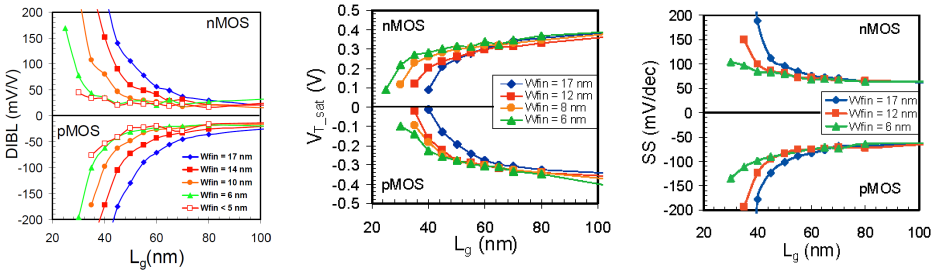
(a) (b)

Figure 1.3: Comparison of single and double gate devices. (a) Comparison of of DIBL[25]. (b) Comparison of sub-threshold swing[25].

swing [24][25][21][32]. Fig. 1.3 compares DIBL and sub-threshold swing for single gate and double gate devices. It can be seen that both the DIBL and subthreshold swing are improved by using the double gate structure. As a depleted-substrate transistor [7], FinFET can overcome the continue scaling obstacles [17]. Recently Intel [19] announced its 22nm FinFET process will be used for the next generation processor. IBM is also spending a lot of R&D efforts in FinFET [24].

There are mainly three kinds of FinFET fabrication techniques[2][7]:

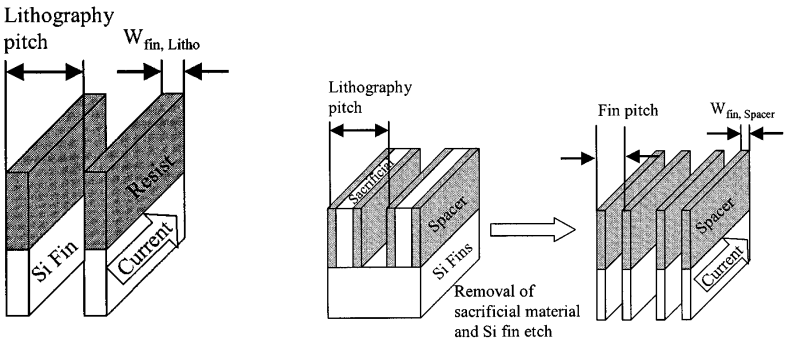
3-Terminal (3T) FinFET, 4-Terminal (4T) FinFET and Mix-FinFET. In this thesis the main focus is 3T FinFET.



(a) (b) (c)

Figure 1.4: SCE for different fin width[33]. (a)DIBL as a function of gate length for various fin width. (b)Saturated threshold voltage with gate length at $V_D = 1V$ for various fin width. (c)Sub-threshold slope at $V_D = 1V$ for various fin width.

The three-dimensional 3T FinFET graph and its corresponding top view are in Fig. 1.1. The photos taken by scanning electron microscope (SEM) show the real fabricated FinFET in Fig. 1.2. It can be seen that a single strip is used to implement both front and back gates for all fins. The single strip structure makes FinFET layout density close to that of a traditional CMOS [3][2]. The difference between 3T FinFET and traditional CMOS is obvious. The active region between drain and source in CMOS is connected together in one rectangular shape, while the channel of FinFET is covered in both sides by the three-dimensional double gate structure.



(a) (b)

Figure 1.5: Fin density caparison[9]. (a)Conventional lithography. (b)Spacer patterning technology.

1.2 FinFET Manufacturing Challenges

FinFET manufacturing issues have been studied by both the academic and the industry for many years [11]. A large number of papers and patents have been published.

To begin with, the manufacturability of the fin width has been a challenge for many years. Research has shown that scaling the fin width can improve device's immunity to short channel effects [33]. As shown in Fig. 1.4, DIBL, saturated threshold voltage and sub-threshold slop are improved by scaling the fin width. Previous work has been done to solve the fin width scaling problem [9][10][8]. The technology called spacer patterning plays an essential role in manufacturing small width fins. This technique uses a sacrificial layer and a chemical vapor deposition(CVD) layer. The sub-7nm structure is achieved by conventional dry etching at the CVD sacrificial layer. The mini-

mum feature size is limited by the CVD film thickness instead of the feature size of optical or e-beam lithography. People have proposed double patterning or quadric patterning technique to improve the fin density. Fig. 1.5 shows the doubling of fin density by using spacer technique. The double patterning technique is an example to understand the detailed manufacturing process. First the SiGe is deposited by LPCVD as a sacrificial layer. Then optical lithography etch is used to get pattern on sacrificial layer which serves as a foundation to form the spacers. After that, spacer is deposited around the patterned sacrificial layer by CVD to act as a hard mask (HM) during the direct etch step. Then the SiGe sacrificial layer is selective removed. The direct etch achieves the Si fin patterning by only preserving the Si under the HM. Finally, the HM is selectively removed. The fin width is determined by the thickness of the HM, which corresponds to the thickness of CVD process. The gate, drain and source are fabricated afterwards using selective epitaxial growth (SEG). In order to further increase the fin density, quadric patterning can be added during the above process. Quadric patterning uses the first sacrificial spacer as a sidewall to grow the second sacrificial layer, which serves as the HM for the directly etch [30].

The second challenge is the lithography variation during the manufacturing process. Due to the limitations of the image system, a large number of variations are introduced during the manufacturing process [31][29][5]. As shown in Fig. 1.6, the variations occurred during lithography process can cause performance degradation or even functional failure. Many methods have been

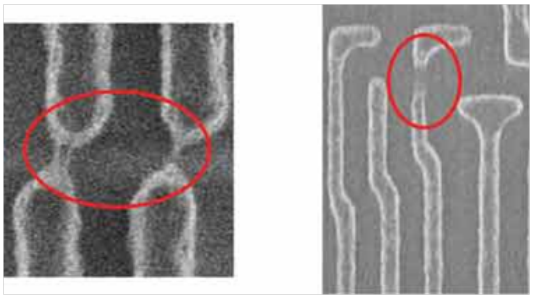


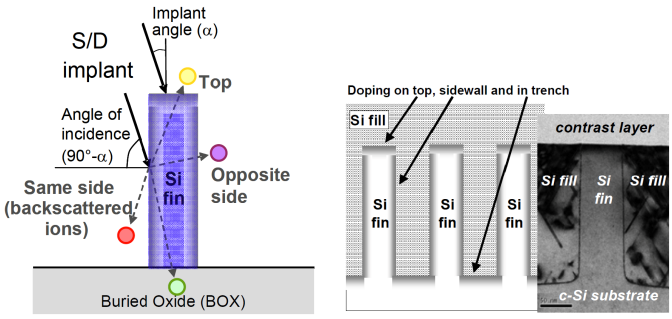
Figure 1.6: Variation in deep submicron technology[1]

proposed to measure the quality of the lithography. This thesis uses the edge placement error (EPE) to characterize the robustness of the layout after lithography process. EPE is defined as the difference between the ideal drawn layout shape and the real fabricated shape. This thesis considers the EPE at metal one layer, because metal one layer is the only metal layer at the standard cell level. Many previous works have been done for the definition of EPE. For instance, Eq. 1.1 is from one of the latest works[15] about the statistical characterization of the EPE using linear regression method.

$$EPE = -14d^3e^2 + 54d^2e^2 - 72de^2 + 57d^3e - 257d^2e + 331de + 4e^2 - 17e - 6d^3 - 102d^2 + 119d - 0.00015w + 0.0015e + 0.0086 \quad (1.1)$$

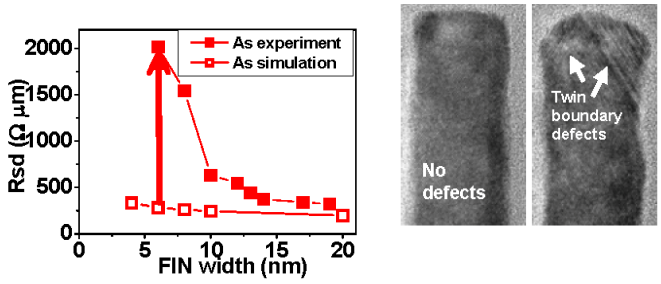
Where d is the defocus factor, e is the exposure parameter, w is the gate width and e is the field extension.

Another challenge for FinFET is the junction formation issue. The definition of the α is shown in Fig. 1.7(a). As shown in Fig. 1.7(b), highly



(a) (b)

Figure 1.7: Junction formation[20]. (a)Implantation angle definition. (b)Doping at different position.



(a) (b)

Figure 1.8: Manufacture issue for small fin width[28]. (a)R_{sd} with different fin width. (b)Defect picture in SEM.

tilted implants are required to incorporate the dopants along the fin. Among all the implantation, only a fraction is retained. The amount of the retained implantation has a strong relationship with the implant angle α [12]. With the increasing of the fin height and the reducing of the fin pitch, the implantation angle is reduced to avoid shadowing effect. By reducing the implantation angle, sidewall and trench are more effectively doped. However, the reduction in implant angle increases the backside scattering and leads to great loss

in implantation dose. In order to solve this problem, pulsed plasma doping (PLAD) has been proposed[22]. Although PLAD can relieve the implantation dose loss problem, it brings full amorphization and recrystallization problems while manufacturing thin and tall fins. Moreover, the recrystallization during the post-implant anneal process as well as the implant damage during the heavy ion doping process will increase the drain-source access resistance. As shown in Fig. 1.8, when the fin width decreases, the recrystallization and drain-source access resistance increase obviously. This undesirable effect will bring problems to both the reliability and the performance of the device.

Chapter 2

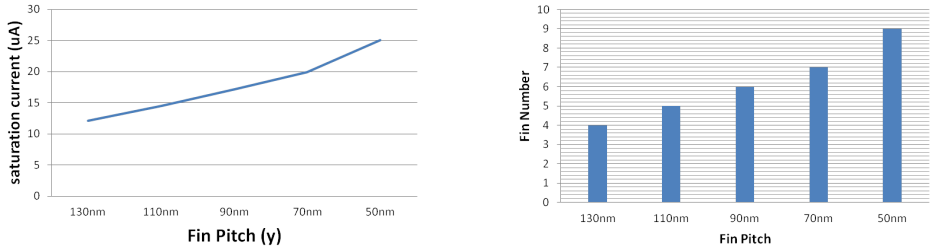
FinFET Standard Cell Characterization

There are many variables in FinFET physical design that can be optimized. This thesis includes the metal pitch x, the fin pitch y, and the fin width w as design variables for characterization and optimization. This chapter explores the impact of metal pitch on average EPE and leakage current. The impact of fin pitch on leakage current and implantation angle. The impact of fin width on saturation current, leakage current and the implantation angle. Finally, these factors are linked with the standard cell performance. The predictive technology model for FinFET [18] is used in this thesis.

2.1 Fin Pitch Characterization

Fin pitch affects both the saturation current and the implantation angle. The implantation angle will be modeled in the next section. This section only considers the impact of fin pitch on saturation current.

Some previous works have been done in modeling the saturation current for standard cell design optimization [37][36][4]. Although they use traditional CMOS instead of FinFET, the device simulation tools used in these papers are three-dimensional simulation tools such as TCAD. Three-dimensional simula-



(a) (b)

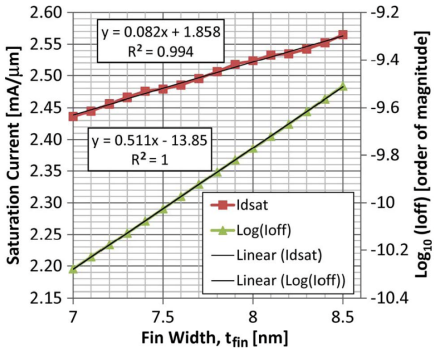
Figure 2.1: Fin pitch relation with. (a)Saturation current. (b)Fin number.

tion will give more accurate results, but the computation complexity makes it more time-consuming. Instead of using three-dimensional simulation, this thesis uses hspice to build a two-dimensional environment to do the characterization. It is assumed that the fin pitch is the same for all the fins in a certain device. Compared with traditional CMOS, fin pitch is a unique parameter for FinFET. The saturation current for different fin pitch is shown in Fig. 2.1(a). It can be seen that the saturation current increases as the fin pitch becomes smaller. The reason is that reducing the fin pitch creates more available space along the vertical direction of the device. During the characterization process, the additional space is used to increase the number of fins. The fin number for different fin pitch is shown in Fig. 2.1(b). It can be seen that the fin number increases as the fin pitch scales down. The increasing of the fin number becomes more obvious under small fin pitch values. This phenomenon is also reflected in the saturation current. It can be seen that there is a sharp improvement under small fin pitch values.

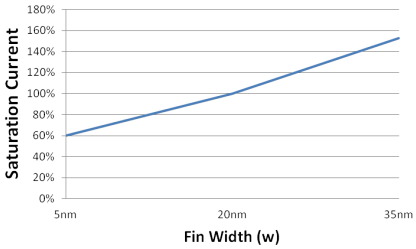
2.2 Fin Width Characterization

The fin width has impact on saturation current, leakage current and implantation angle. Previous works have been done about fin width dependence for saturation current and the leakage current [27][23][35][13][13][14]. Results have shown that scaling the fin width brings better SCE control. This, however, accompanied by an on-stage drive current degradation. Ion implantation is a general way to introduce dopants to the silicon, but amorphization may be caused at the same time when highly doped source-drain region is formed. If the recrystallization after amorphization happens on thin silicon body, the crystalline integrity becomes worse as the fin width is scaled. These effects lead to minor reduction in saturation current. The saturation current and leakage current for different fin width is shown in Fig. 2.2(a), which is further extended to a wider range of fin width values, taking $w = 20nm$ as the original point. Pise-wise linear approximation is used for the leakage current during the extend process. The extended results for saturation current and leakage current is shown in Fig. 2.2(b) and Fig. 2.2(c). It can be seen that as the fin width varies from 5nm to 35nm, the delta saturation current varies from sixty percents to one hundred and fifty percents. At the same time, the leakage current varies from five percents to six hundred percents.

It is mentioned before that small implant angle may bring manufacturability issues, including fin recrystallization, higher source drain contact resistance and PLAD damage. Therefore, it is more desirable to have a bigger implantation angle. The implantation angle is determined by three variables.



(a)



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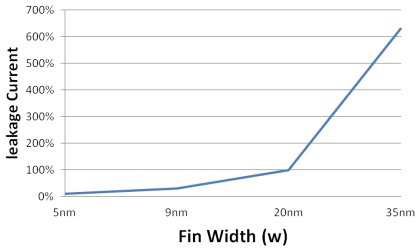


(c)

Figure 2.2: Fin width and current. (a)Saturation and leakage current under different fin pitch[27]. (b)Extended relationship for saturation current. (b)Extended relationship for leakage current.

We draw the cross section graph in in Fig. 2.3 to illustrate the definition of the implantation angle. The maximum possible implantation angle θ should guarantee the top, sidewall and trench are all effectively doped. Further increasing of the implantation angle will make it difficult for part of the sidewall to be effectively doped. The expression of the implantation angle θ can be derived from the figure:

$$\theta = tan^{-1}\left(\frac{y-w}{h}\right) \tag{2.1}$$

Where w is the fin width, y is the fin pitch, h is the height of the fin. The FinFET model in this thesis is two-dimensional instead of three-dimensional, so the maximum value of y y_{max} is used as the value of h during optimization.

2.3 Metal Pitch Characterization

The metal pitch x has impact on both average EPE and leakage current. During the optimization process, metal pitch is the only variable affects average EPE. An environment based on Calibre Workbench is built to measure the relationship between the metal pitch and the average EPE. As shown in Fig. 2.4, the metal one strip after lithography is different from the original drawing. The original standard rectangular shape turns into the irregular polygon shape. This is due to various variation factors during the lithography process. The average EPE simulation results for different metal pitch value is shown in Fig. 2.5. The average EPE is the average of all the EPE value reported by the simulation environment. The unit of average EPE is nm. It can be seen that when metal pitch reduces, the average EPE first increases. Beyond some threshold value of x, the average EPE remains the same. The similar effect can be seen for the max EPE. Average EPE will be used as a metric during the optimization process.

Metal pitch also affects leakage current. The leakage current for differ-

ent metal pitch is measured with the parasitic extracted netlist from Hspice. As shown in Fig. 2.6, the leakage current increases as the metal pitch decreases. This is due to the fact that the entire fin length, including the portion under the gate and the portion that is not under the gate, decreases when the metal pitch decreases. The reduced fin length makes it easier for the leakage current to flow.

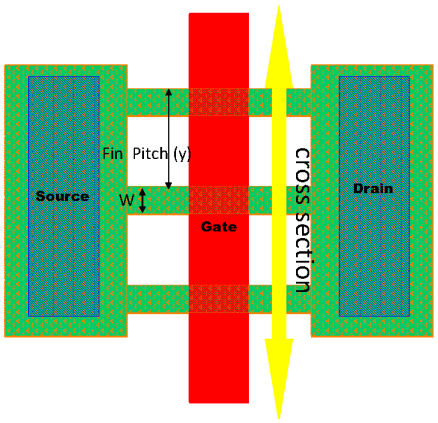
2.4 Standard Cell Performance Characterization

Both combinatorial cells and sequential cells are included in the standard cell library, including inverter, 2-input NAND gate, 2-input NOR gate and the D flip-flop. Hspice is used to characterize the propagation delay and leakage current. Calibre workbench is used to characterize average EPE.

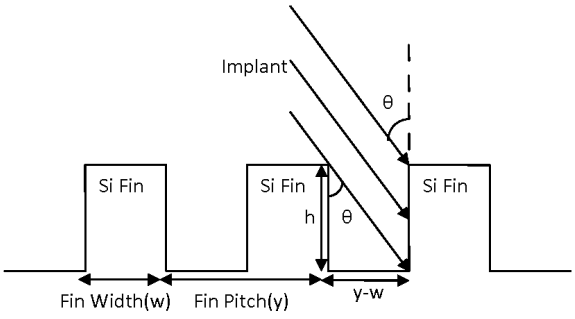
The characterization result is shown in Table 2.1. It is assumed that ${EPE_{avg}}^{M1}$ of the standard cell is the ${EPE_{avg}}^{M1}$ of the unit width transistor times the sum of the gate size of that cell. The unit is still in nm. For example, the inverter is considered to be composed of a width 2 pFET and a width 1 nFET, so the ${EPE_{avg}}^{M1}$ is three times that of the unit width transistor. The original values for all the physical design variables are: $w = 20nm, y = 110nm, x = 140nm$.

Table 2.1: Standard Cell Characterization

Cell	Original Design					
	Delay(ps)	$I_{leak}\,(nA)$	$EPE_{avg}{}^{M1}\,(nm)$	$T_{setup}\,(ps)$	$T_{hold}\,(ps)$	θ
INV	14.1	9.9	15.6	-	-	
NAND2	10.2	20.9	41.6	-	-	
NOR2	21.7	29.7	52	-	-	39^o
DFF	28.1	387	405.6	24.9	7.6	

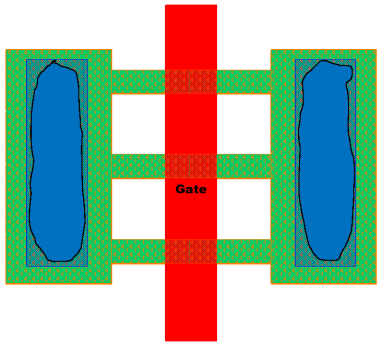


(a)

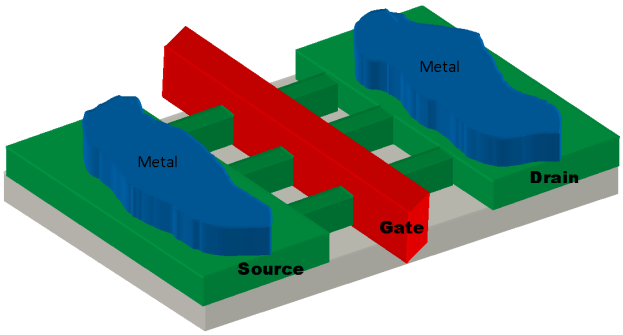


(b)

Figure 2.3: Implantation angle. (a)Cross section position. (b)Cross section view with y and w.

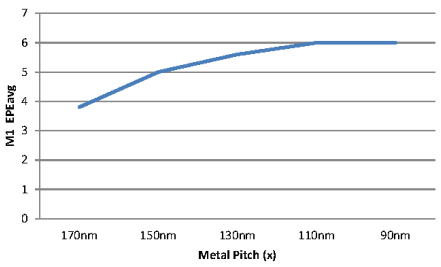


(a)

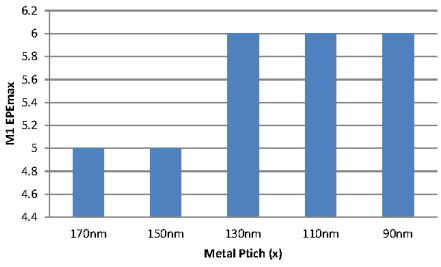


(b)

Figure 2.4: Metal one layer EPE. (a)Two-dimensional view. (b)Three dimensional view.



(a)



(b)

Figure 2.5: Metal one layer EPE . (a)Average EPE. (b)Maximum EPE.

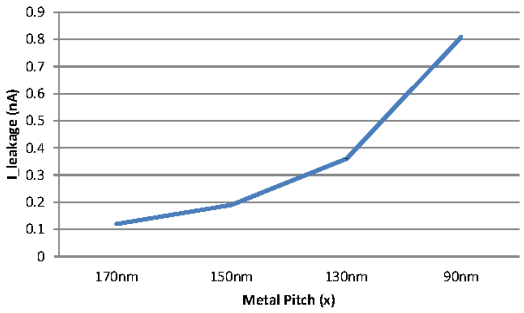


Figure 2.6: Leakage current under different fin pitch

Chapter 3

Problem Formulation and Optimization Results

3.1 Problem Formulation

This section focus on the formulation of objective function as well as the constrains. Although the problem formulation for combinatorial cells is slightly different from that of the sequential cells, most of the parameters are the same. The problem formulation listed below is for sequential cells. The problem formulation for combinatorial cells can be easily derived by removing the setup time and the hold time parameters. Four metrics are included to judge the quality of the physical design. A weighted summation of the four metrics is used as the objective function. As shown in Eq. 3.1, the goal is to maximize the saturation current and the implantation angle, while minimize the leakage current and the average EPE.

$$
\begin{aligned}
\max \quad & \alpha I_{dsat} - \beta {EPE_{avg}}^{M1} - \gamma I_{leak} + \lambda\theta \qquad (3.1)\\
\text{s.t.} \quad & {EPE_{avg}}^{M1} \leq {EPE_{avg}}^{M1}{}_{th}\\
& I_{dsat} \geq (I_{dsat})_{th}\\
& I_{leak} \leq (I_{leak})_{th}\\
& \theta \geq \theta_{th}\\
& T_{setup} \leq (T_{setup})_{th}\\
& T_{hold} \leq (T_{hold})_{th}\\
& {EPE_{avg}}^{M1} = f_{EPEavg}(x)\\
& T_{setup} = f_{setup}(I_{dsat})\\
& T_{hold} = f_{hold}(I_{dsat})\\
& I_{dsat} = f_{Idsat}(y, w)\\
& I_{leak} = f_{Ileak}(x, w)\\
& \theta = f_{\theta}(y, w)
\end{aligned}
$$

Where $\alpha, \beta, \gamma, \lambda$ are the weights of saturation current, average EPE, leakage current and implantation angle. The unit of the saturation current is uA. The unit of the leakage current is nA. The unit of the implantation angle is degree. The initial values of the four weights are: $\alpha = 8, \beta = 2.8, \gamma = 159, \lambda = 1$. The initial values of the four metrics are set to equal the weight. The weights are changed later according to different optimization scenarios. ${EPE_{avg}}^{M1}{}_{th}$ is the maximum average EPE limitation to guarantee the yield of the design. $(I_{dsat})_{th}$

is the minimum saturation current limitation to guarantee the performance of the standard cells. $(I_{leak})_{th}$ is the maximum leakage current limitation to guarantee the leakage power consumption of the standard cells. θ_{th} is the minimum implantation angle to guarantee no essential damage during the implantation process. $(T_{setup})_{th}$ and $(T_{hold})_{th}$ are the setup and hold time design specifications that must be satisfied for the D flip-flop. ${EPE_{avg}}^{M1}$ is a function of the metal pitch. I_{dsat} is a function of the fin pitch as well as the fin width. I_{leak} is a function of both the metal pitch and the fin width. θ is a function of both the fin pitch and the fin width.

In the above problem formulation, there are many functions of two variables. It is assumed that both variables are independent from each other. Leakage current function is used as an example to illustrate this, which is shown in Eq. 3.2. One thing need to be pointed out is although the implantation angle is also determine by two variables, the Eq.2.1 has shown that both x and w will be calculated together to derive the θ.

$$I_{leak} = f_{Ileak}(x, w) = I_{leak}(x) \times (1 + \Delta I_{leak}(w)) \tag{3.2}$$

3.2 Optimization Results

In order to show the universal solution for general objective functions, we implement an exhaustive algorithm in Matlab to solve this problem. The exhaustive algorithm is shown in Algorithm 1. In the algorithm we use F_{obj}

to represent the objective function in Eq.2.1. Due to the limited solution space, the runtime is within two seconds. The optimization results are shown in Table 3.1 and Table 3.2. There are two different optimization objective functions. The first one is performance driven, which pushes the optimization of saturation current and leakage current to the limit. This is achieved by setting higher weights to saturation current and leakage current in the objective function. The detail weights for performance driven optimization is $\alpha = 8, \beta = 28, \gamma = 1590, \lambda = 1$. The second one is manufacturability driven, which pushes the optimization of EPE and implantation angle to the limit. This is achieved by setting higher weights to EPE and implantation angle. The detail weights for manufacturability driven optimization is $\alpha = 80, \beta = 2.8, \gamma = 159, \lambda = 10$.

Algorithm 1 Greedy Algorithm for ${EPE_{avg}}^{M1}$ optimization

for each $y_i \in [y_{min}, y_{max}]$ **do**
 for each $x_i \in [x_{min}, x_{max}]$ **do**
  for each $w_i \in [w_{min}, w_{max}]$ **do**
   if all the constrains are satisfied **then**
    if $F_{obj}(x_i, y_i, w_i) \geq (F_{obj})_{max}$ **then**
     set $x_{final} = x_i, y_{final} = y_i, w_{final} = w_i$
     set $(F_{obj})_{max} = F_{obj}(x_i, y_i, w_i)$
    endif
   endif
  endfor
 endfor
endfor
return $x_{final}, y_{final}, w_{final}$

Table 3.1: Performance Driven Optimization Results

Cell	Performance Driven, Optimize Delay and leakage					
	Delay(ps)	$I_{leak}\,(nA)$	${EPE_{avg}}^{M1}\,(nm)$	$T_{setup}\,(ps)$	$T_{hold}\,(ps)$	θ
INV	19.8	0.83	11.7	-	-	
NAND2	14.3	1.75	31.2	-	-	
NOR2	30.5	2.51	39	-	-	35^o
DFF	39.5	32.31	304.2	25.2	7.9	

Table 3.2: Manufacturability Driven Optimization Results

Cell	Manufacturability Driven, Optimize ${EPE_{avg}}^{M1}$ and θ					
	Delay(ps)	$I_{leak}\,(nA)$	${EPE_{avg}}^{M1}\,(nm)$	$T_{setup}\,(ps)$	$T_{hold}\,(ps)$	θ
INV	20.4	2.97	11.4	-	-	
NAND2	14.8	6.27	30.4	-	-	
NOR2	31.5	8.91	38	-	-	41^o
DFF	40.7	116.1	296.4	25.3	7.9	

Chapter 4

Conclusion

The results show that the performance driven optimization effectively reduces the delay and the leakage current, which brings significant enhancements to the performance of the standard cells. At the same time, the average EPE layer and implantation angle are compromised. The manufacturability driven design greatly reduces the average EPE and improves the implantation angle, which is very beneficial for yield. At the same time, the design endures larger leakage current and delay. Essentially, the results illustrate the trade off between performance and manufacturability.

Further pushing the saturation current of flip-flops leads to the reduction of delay, which will relax the latest required arrival time for the previous pipeline stage while relax the earliest required arrival time for pipeline stage after the flop. Although other methodologies such as low threshold voltage cell swapping and clock cycle borrowing can be used to achieve timing closure, they may increase the mask cost or the design complexity. Therefore, a flop swapping methodology can be used to provide potential help for all the critical paths to meet timing without additional mask cost or design complexity. This methodology can be easily implement in the design flow by adding some low

metal pitch and fin pitch cells. This kind of standard cells will be used by the CAD tools during the latest timing closure stage. One thing need to be pointed out is that this kind of swapping can not be used abusively in the design, because essentially it is a trade off between speed and yield.

In conclusion, characterization of the FinFET standard cell design is done. The performance and manufacturability optimization results are attained. The optimization results show the tradeoff between performance and manufacturability.

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Vita

Boyang Zhang was born in Xi'an, China in 1988. He received a Bachelor degree from Xi'an Jiaotong University. In Fall 2010, Boyang enrolled in the masters program in the Department of Electrical and Computer Engineering at the University of Texas at Austin. In 2011, Boyang joined the Design Automation Lab at the electrical and computer engineering department of University of Texas at Austin.

Permanent address: 7303 Wood Hollow Drive Austin TX, 78731

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